DOCUMENT-IDENTIFIER: US 6151684 A
TITLE: High availability access to input/output devices in a distributed system

BSPR:
Thus, it can be seen that there is a need to define a way in which access to devices can be transparently recovered, that is, rebuilding the internal system software framework to allow some other node in the cluster to assume the role of the controlling entity for the device in such a way that users and applications are not aware that a failure occurred. This has many implications. For instance, the device's state must be preserved so it looks exactly the same as it did, before the failure. The device driver on the new controlling node must have the same state information and be able to process requests in the same manner as the device driver on the failed node. The way in which the user accesses the device must remain exactly the same although the user's requests now have to go to a different node in the cluster. Any requests in transit or on the device at the time of the failure must be analyzed and replayed if necessary. All this and more needs to take place transparently. The combination of the SAN-based system architecture and an SSI distributed operating system provides the basic framework on which a solution for high availability access to I/O devices can be built.

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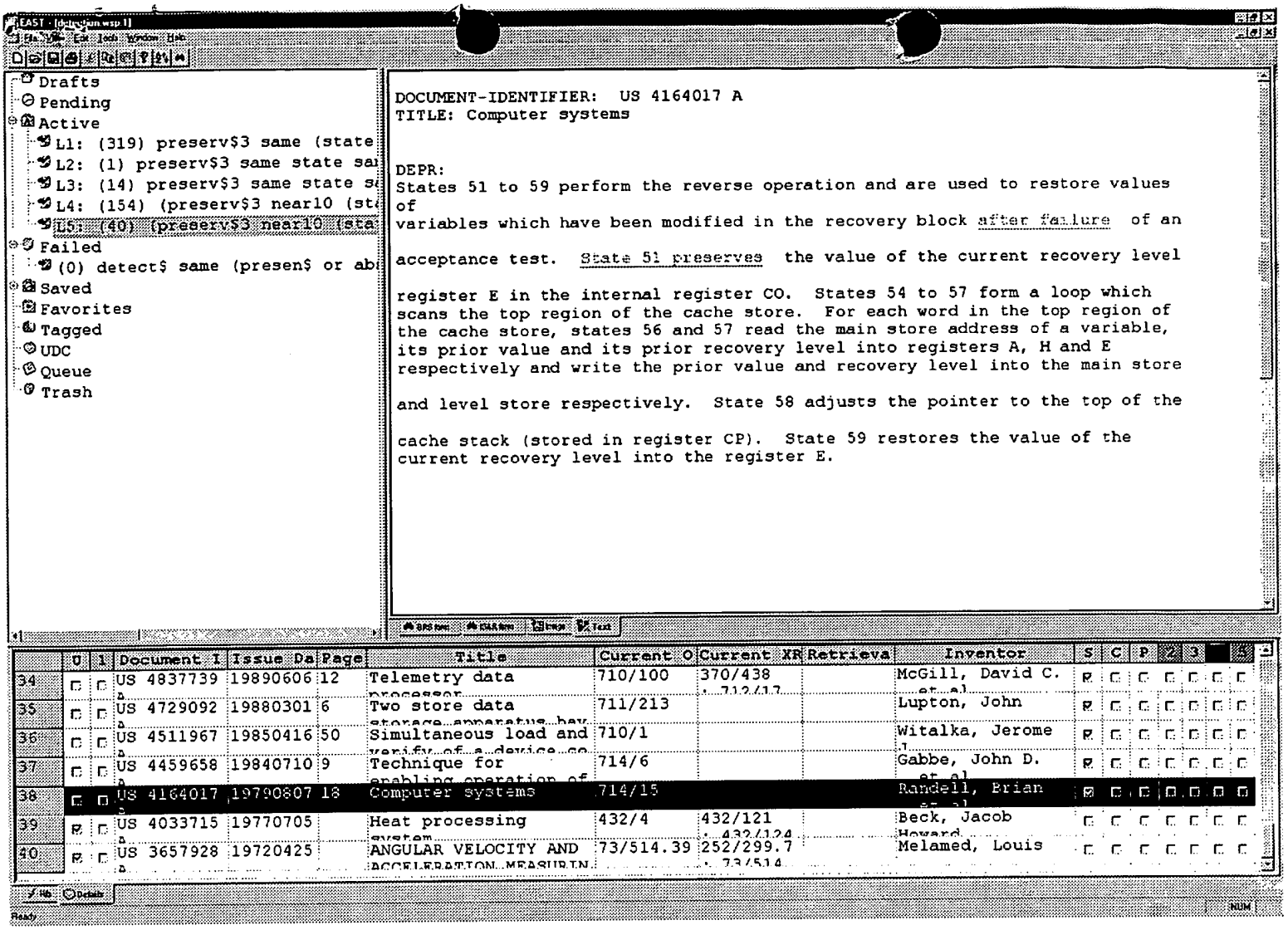
714/4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DOCUMENT-IDENTIFIER: US 4164017 A
TITLE: Computer systems
DEPR:
States 51 to 59 perform the reverse operation and are used to restore values of
variables which have been modified in the recovery block after failure of an
acceptance test. State 51 preserves the value of the current recovery level
register E in the internal register CO. States 54 to 57 form a loop which
scans the top region of the cache store. For each word in the top region of
the cache store, states 56 and 57 read the main store address of a variable,
its prior value and its prior recovery level into registers A, H and E
respectively and write the prior value and recovery level into the main store
and level store respectively. State 58 adjusts the pointer to the top of the
cache stack (stored in register CP). State 59 restores the value of the
current recovery level into the register E.
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34 US 4837739 19890606 12 Telemetry data processor 710/100 370/438 McGill, David C. et al
35 US 4729092 19880301 6 Two store data storage apparatus hav 711/213 Lupton, John
36 US 4511967 19850416 50 Simultaneous load and verify of a device co 710/1 Witalka, Jerome J
37 US 4459658 19840710 9 Technique for enabling operation of 714/6 Gabbe, John D. et al
38 US 4164017 19790807 18 Computer systems 714/15 Randell, Brian et al
39 US 4033715 19770705 Heat processing system 432/4 432/121 Beck, Jacob Howard
40 US 3657928 19720425 ANGULAR VELOCITY AND ACCELERATION MEASURIN 73/514.39 252/299.7 Melamed, Louis
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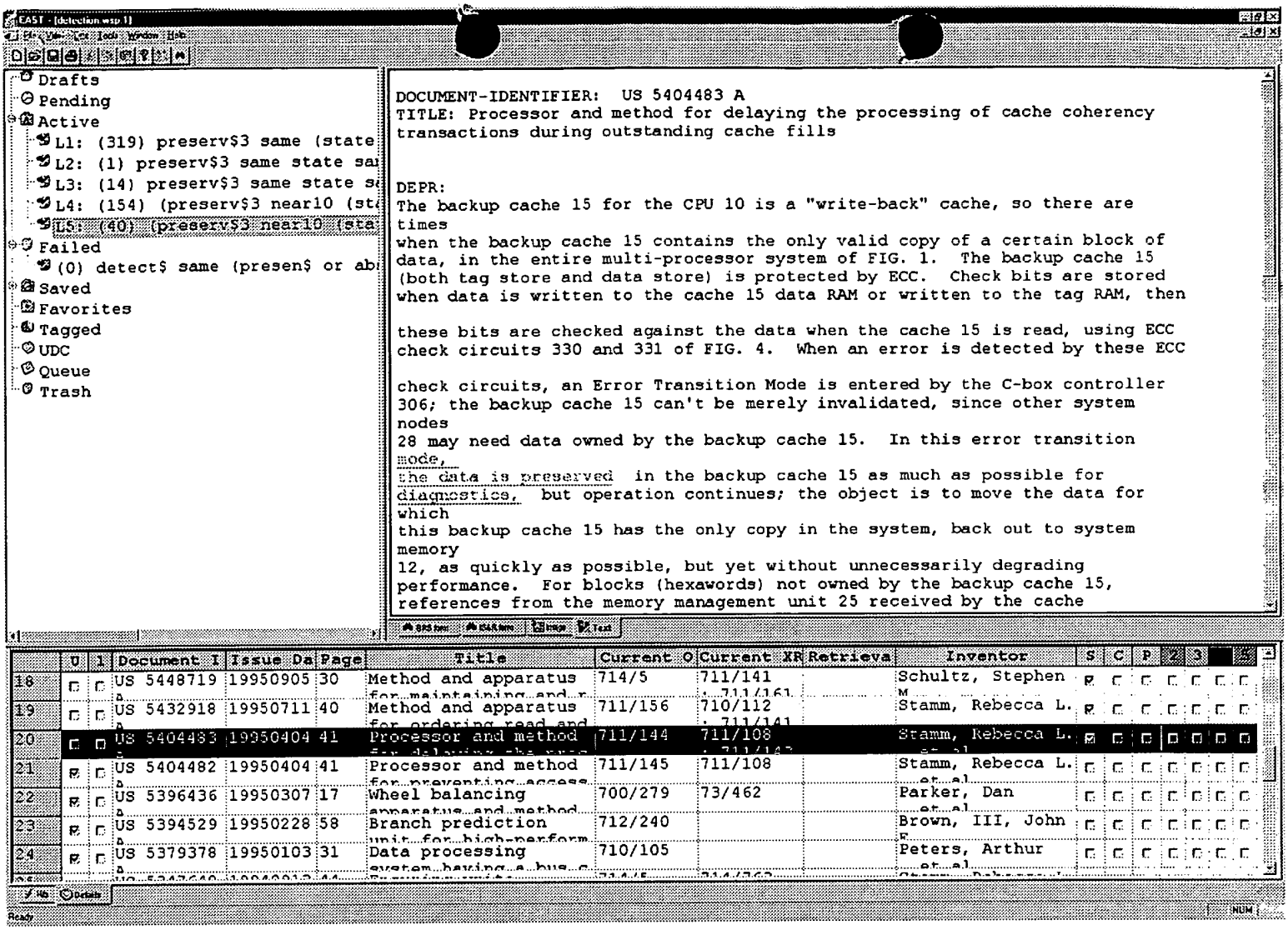
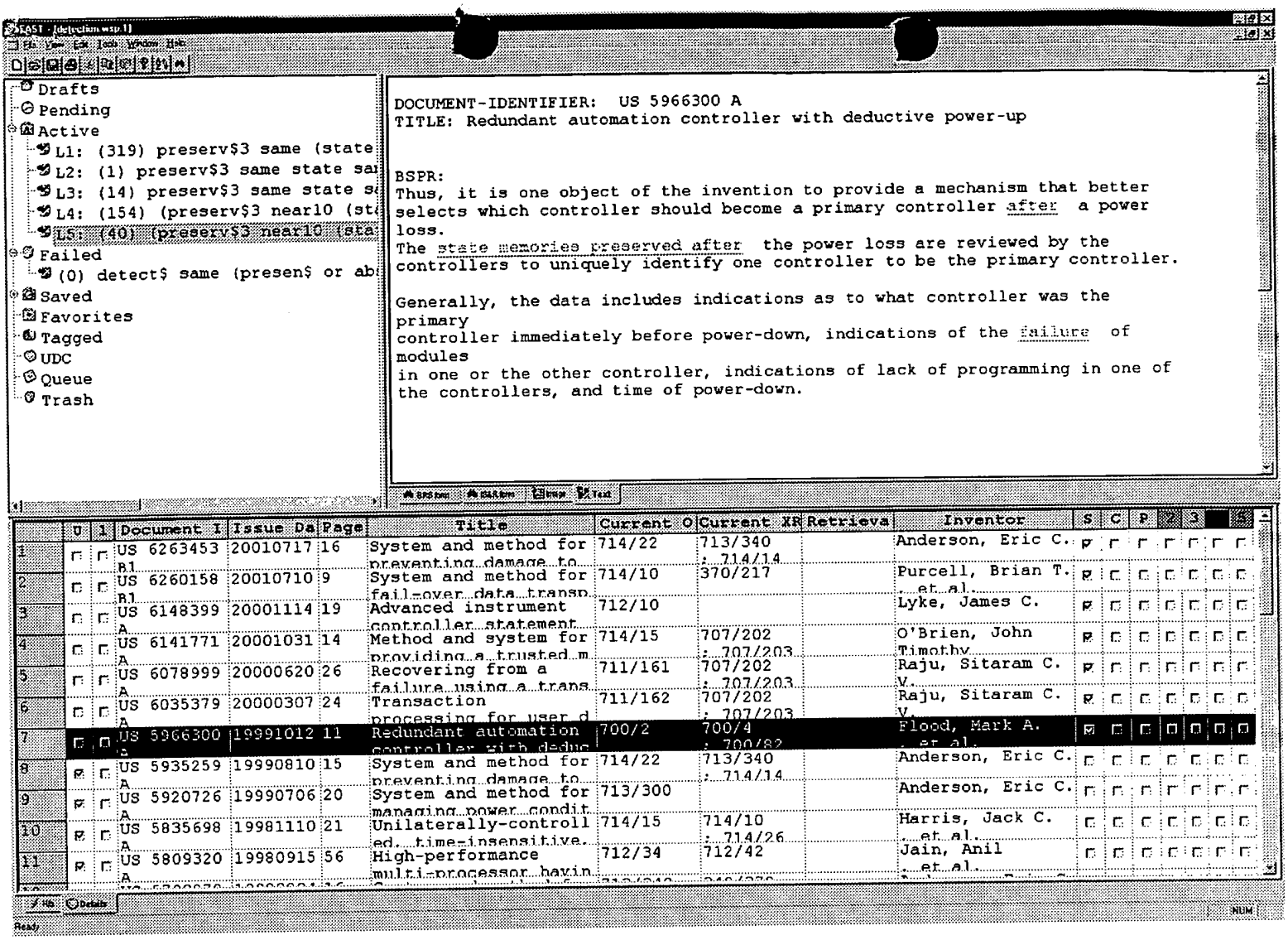


	U	1	Document I	Issue Da	Page	Title	Current O	Current XR	Retrieva	Inventor	S	C	P	2	3
18	☐	☐	US 5448719 A	19950905	30	Method and apparatus for maintaining and r	714/5	711/141 ; 711/161		Schultz, Stephen M	☑	☐	☐	☐	☐
19	☐	☐	US 5432918 A	19950711	40	Method and apparatus for ordering read and	711/156	710/112 ; 711/141		Stamm, Rebecca L.	☑	☐	☐	☐	☐
20	☐	☐	US 5404483 A	19950404	41	Processor and method for delaying the proc	711/144	711/108 ; 711/143		Stamm, Rebecca L. et al	☑	☐	☐	☐	☐
21	☑	☐	US 5404482 A	19950404	41	Processor and method for preventing access	711/145	711/108		Stamm, Rebecca L. et al	☐	☐	☐	☐	☐
22	☑	☐	US 5396436 A	19950307	17	Wheel balancing apparatus and method	700/279	73/462		Parker, Dan et al	☐	☐	☐	☐	☐
23	☑	☐	US 5394529 A	19950228	58	Branch prediction unit for high-perform	712/240			Brown, III, John F.	☐	☐	☐	☐	☐
24	☑	☐	US 5379378 A	19950103	31	Data processing system having a bus c	710/105			Peters, Arthur et al	☐	☐	☐	☐	☐



	0	1	Document I	Issue Da	Page	Title	Current O	Current XR	Retrieva	Inventor	S	C	P	2	3	4	5
1	☐	☐	US 6263453 B1	20010717	16	System and method for preventing damage to	714/22	713/340 ; 714/14		Anderson, Eric C.	☑	☐	☐	☐	☐	☐	☐
2	☐	☐	US 6260158 B1	20010710	9	System and method for fail-over data transp	714/10	370/217		Purcell, Brian T. ..et al.	☑	☐	☐	☐	☐	☐	☐
3	☐	☐	US 6148399 A	20001114	19	Advanced instrument controller statement	712/10			Lyke, James C.	☑	☐	☐	☐	☐	☐	☐
4	☐	☐	US 6141771 A	20001031	14	Method and system for providing a trusted m	714/15	707/202 ; 707/203		O'Brien, John Timothy	☑	☐	☐	☐	☐	☐	☐
5	☐	☐	US 6078999 A	20000620	26	Recovering from a failure using a trans	711/161	707/202 ; 707/203		Raju, Sitaram C. V.	☑	☐	☐	☐	☐	☐	☐
6	☐	☐	US 6035379 A	20000307	24	Transaction processing for user d	711/162	707/202 ; 707/203		Raju, Sitaram C. V.	☑	☐	☐	☐	☐	☐	☐
7	☐	☐	US 5966300 A	19991012	11	Redundant automation controller with deduc	700/2	700/4 ; 700/82		Flood, Mark A. ..et al.	☑	☐	☐	☐	☐	☐	☐
8	☑	☐	US 5935259 A	19990810	15	System and method for preventing damage to	714/22	713/340 ; 714/14		Anderson, Eric C.	☐	☐	☐	☐	☐	☐	☐
9	☑	☐	US 5920726 A	19990706	20	System and method for managing power condit	713/300			Anderson, Eric C.	☐	☐	☐	☐	☐	☐	☐
10	☑	☐	US 5835698 A	19981110	21	Unilaterally-controll ed, time-insensitive,	714/15	714/10 ; 714/26		Harris, Jack C. ..et al.	☐	☐	☐	☐	☐	☐	☐
11	☑	☐	US 5809320 A	19980915	56	High-performance multi-processor havin	712/34	712/42		Jain, Anil ..et al.	☐	☐	☐	☐	☐	☐	☐